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U11

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Ball grid array type semiconductor device, has chips mounted on inner side of U shaped substrate and sealed by resin which is filled between inner surface of substrate and chips

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U14 (2001.03.23) H01L 25/065, H01L 25/07, 25/18

Novelty: Electrode pad (13) is formed on inner surface and connecting terminals (18, 19) are formed on outer surface of flexible insulating substrate (10) which is bent to U shape. Semiconductor chips (11,12) are mounted on inner surface of substrate through the pad in back alignment condition. Resin (16) is filled inside bent substrate between chips to seal the chips.

Use: Ball grid array type semiconductor device.

Advantage: Semiconductor chips are mounted in laminated condition, so improvement in package density of semiconductor chip is achieved. Simplification of mounting operation of semiconductor chip is obtained. When semiconductor device is mounted in substrate, projection configuration of external terminal is not provided outside which chip, so mounting area is reduced. Electrical property of semiconductor device of mounting condition can be examined by performing electrical connection to external terminal arranged to another lateral surface of semiconductor device.

Description of Drawing(s): The figure shows the sectional views of semiconductor device. (Drawing includes non-English language text).

Insulating substrate 10

Semiconductor chip 11,12

Electrode pad 13

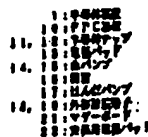
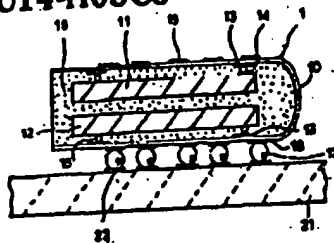
Resin 16

External connecting terminal 18,19

(6pp Dwg.No.1/5)

N2002-022197

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PATENT ABSTRACTS OF JAPAN

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(71)Applicant : NEC CORP

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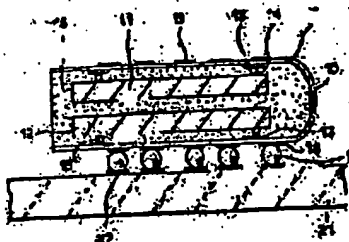
(72)Inventor : HASHIMOTO KATSUMASA

(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device, in which mount density of a semiconductor chip is enhanced, mounting of the semiconductor chip is simplified, and mounting with a solder bump is possible.

SOLUTION: A semiconductor device 1 is provided with an insulating substrate 10, in which an electrode pad 13 is formed on one surface, and external connecting terminals 18 and 19 are formed on the other surface, and two semiconductor chips 11 and 12 mounted on the electrode 13 on one surface of the substrate 10. This device is constituted by folding the substrate 10 to form a U-shape in the direction of the thickness with one surface inward to arrange two semiconductor chips 11 and 12 back to back, and by filling a resin 16 between the folded substrate 10 to seal the semiconductor chips 11 and 12. When the semiconductor device 1 is mounted on a mother board 21, two semiconductor chips 11 and 12 are mounted in a state such that they are laminated. Thus, the mount density of the semiconductor chips to the mother board 21 is improved.



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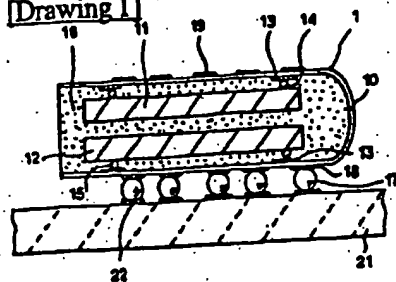
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precisely.

2.*** shows the word which can not be translated.

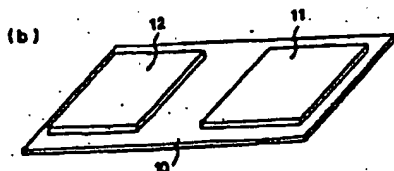
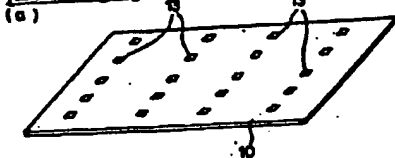
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Drawing 1]



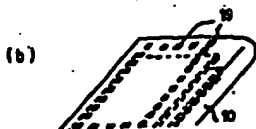
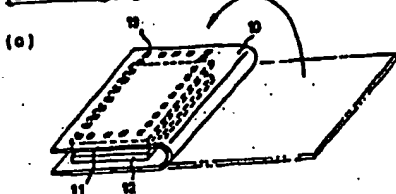
- 1: 半導体装置
10: PPC基板
11: 12: 半導体チップ
13: 基板パッド
14: 15: 金バンプ
16: 銅層
17: はんだバンプ
18: 19: 外部接続端子
20: マザーボード
21: 22: 空気用配線パッド

[Drawing 2]



11. 10: PPC装置
12: 平帯体サブ
13: 電板バッド

[Drawing 3]



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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the semiconductor device which aimed at especially improvement in packaging density about the semiconductor device which carried two or more chips.

[0002]

[Description of the Prior Art] In recent years, improvement in the packaging density of a semiconductor device is demanded, and in order to realize this, the semiconductor device which carried two or more chips as one package is proposed. Drawing 5 is the cross section showing the conventional example of this kind of semiconductor device. The example of drawing 5 (a) carries a semiconductor chip 102, 103 in both sides of a leadframe 101, respectively, connects each semiconductor chip 102, 103 and a leadframe 101 by the bonding wire 104, and carries out package closure with the mould resin 105. Moreover, drawing 5 (b) connects each semiconductor chip 202, 203 to a leadframe 201, after pasting up the tooth back of two semiconductor chips 202, 203 directly, and it carries out package closure with the mould resin 205. After forming a part of leadframe 301 or the whole so that it may become two-step composition, two semiconductor chips 302, 303 are carried in the height position where leadframes differ, it connects with a leadframe 301 directly like illustration of each semiconductor chip 302, 303, or drawing 5 (c) connects by the bonding wire outside drawing, and performs mounting to a mother board 304. Furthermore, drawing 5 (d) carries two semiconductor chips 402, 403 in a substrate 401 at a laminating state, and after connecting each semiconductor chip 402, 403 and a substrate 401 by the bonding wire 404, it carries out package closure with the mould resin 405. Moreover, the solder bump (BGA) 406 is arranged in the rear face of a substrate 401 as an external end-connection child.

[0003] In such a conventional semiconductor device, since the leadframe is used for the semiconductor device of drawing 5 (a) and (c), a leadframe is projected by the way outside a semiconductor chip, the component-side product of a semiconductor device becomes large as compared with the area of a semiconductor chip, and high density assembly becomes difficult. Moreover, in the semiconductor device of drawing 5 (a), (c), and (d), after carrying a semiconductor chip in a laminating state, it is necessary to make connection to wirebonding or a leadframe to each semiconductor chip, and connection will become difficult. Furthermore, in recent years, when the semiconductor device in which mounting by the solder bump is possible like BGA is required, it becomes difficult to adopt structure like drawing 5 (a) - (c). Although it is possible with this point and the structure of drawing 5 (d), with this structure, it is conditions that an upper semiconductor chip is smaller than a lower thing, and it is difficult to realize at two semiconductor chips of the same size.

[0004] The purpose of this invention attains simplification of the loading work of a semiconductor chip, and offers the semiconductor device which moreover enabled mounting by the solder bump while it aims at improvement in packaging density.

[0005]

[Means for Solving the Problem] The insulating substrate to which an electrode pad is formed in one field, and the semiconductor device of this invention has the flexibility in which the external end-connection child connected to the aforementioned electrode pad was formed in the field of

another side in it. It has two semiconductor chips carried in the aforementioned electrode pad in aforementioned one field of the aforementioned substrate. While turning aforementioned one field inside, bending the aforementioned substrate to a U character type in the thickness direction and constituting the two aforementioned semiconductor chips in the very close state, it is characterized by having been filled up with the resin between the substrates bent the account of before, and closing the aforementioned semiconductor chip. Here, the aforementioned semiconductor chip is carried according to flip chip structure to the aforementioned electrode pad. Moreover, the aforementioned external end-connection child is arranged in one [at least] near lateral surface of the field of the outside of the aforementioned substrate bent by the described [above] U character type. In this case, the aforementioned external end-connection child is arranged in the lateral surface by the side of both above of the aforementioned substrate, respectively, and it is desirable [the child] that the solder ball for constituting ball grid array structure to the external end-connection child by the side of one superficies is connected while electrical connection of each aforementioned external end-connection child is carried out to the aforementioned semiconductor chip, respectively.

[0006] According to this invention, a semiconductor device is constituted where a laminating is mutually carried out because two semiconductor chips carried in the insulating substrate bend a substrate to a U character type and form it. Therefore, when a semiconductor device is mounted, two semiconductor chips will be mounted where a laminating is carried out, and its packaging density of the semiconductor chip to a mounting substrate improves. Moreover, since the external end-connection child of a semiconductor device was arranged in one [at least] lateral surface of the lateral surface of the substrate bent to the U character type, while becoming possible to mount an external end-connection child with solder bump structure, when a semiconductor device is mounted in a mounting substrate, an external end-connection child projects to a way outside a semiconductor chip, is not stationed, and can reduce a component-side product.

[0007] [Embodiments of the Invention] Next, the operation gestalt of this invention is explained with reference to a drawing. Drawing 1 is the cross section of 1 operation gestalt of the semiconductor device 1 of this invention. In the aforementioned semiconductor device 1, two semiconductor chips 11 and 12 are connected to the whole surface of the FPC substrate (flexible printed circuit board) 10 which consists of material with flexibility, such as polyimide resin, by the flip-chip-bonding method. That is, the electrode pad 13 which consisted of ***** is formed in one field of the FPC substrate 10, and the golden bumps 14 and 15 prepared in the electrode of each semiconductor chips 11 and 12, respectively are connected to the aforementioned electrode pad, respectively. Moreover, the aforementioned FPC substrate 10 is mostly bent by the U character type in the thickness direction in the mid-position so that the two aforementioned semiconductor chips 11 and 12 may be faced. And it fills up with the closure resin 16 between the inside space where the aforementioned FPC substrate 10 was bent, i.e., the aforementioned semiconductor chips 11 and 12 and the FPC substrate 10, and the aforementioned semiconductor chips 11 and 12 are closed between the FPC substrates 10. Moreover, the external end-connection children 18 and 19 constituted from ***** by the superficies of the aforementioned FPC substrate 10 like the aforementioned electrode pads 14 and 15 are arranged, and globular form solder BAMBU 17 is connected to the external end-connection child 18 of the superficies of the illustration bottom of the FPC substrate 10, and it is constituted here as an external terminal of BGA (ball grid array) structure. Moreover, the external end-connection child 19 of the superficies of an illustration top is formed in electrode pad structure. The aforementioned semiconductor device is constituted as CSP (chip-size package) by such composition.

[0008] Drawing 2 and drawing 3 are the outline perspective diagrams for explaining the manufacture method of the semiconductor device 1 of drawing 1. Like drawing 2 (a), the FPC substrate 10 is formed in the shape of [of the rectangle of the size which can arrange two semiconductor chips] sheet metal, and the electrode pad 13 for carrying a semiconductor chip with electric conduction foils, such as copper foil, is arranged in the upper surface of the FPC substrate 10 which consists of insulating materials, such as polyimide resin. In addition, the wiring

and the through hole to which each aforementioned electrode pad 13 abbreviated illustration -- mutual -- or it connects with the external end-connection children 18 and 19 of the rear face of the FPC substrate 10 moreover, the wiring outside drawing described above in the inferior surface of the tongue of the aforementioned FPC substrate 10 as shown in drawing 1 and a through hole -- the aforementioned electrode pad 13 -- or the aforementioned external end-connection children 18 and 19 of the electrode pad structure by which electrical connection was carried out mutually are arranged

[0009] Subsequently, two semiconductor chips 11 and 12 are carried in the upper surface of the aforementioned FPC substrate 10 like drawing 2 (b). The golden bumps 14 and 15 (refer to drawing 1) are formed in the electrode prepared in the inferior surface of tongue of illustration, respectively, and each semiconductor chips 11 and 12 are connecting these golden bumps 14 and 15 to the electrode pad 13 of the upper surface of the aforementioned FPC substrate 10, and carry semiconductor chips 11 and 12 in the FPC-substrate 10 according to flip chip structure. As this flip chip structure, it is good also as connection structure by the golden-golden sticking-by-pressure method or different direction conductive resin.

[0010] Further, the aforementioned FPC substrate 10 is bent to a U character type in the thickness direction in the simultaneously mid-position like drawing 3 (a), and it forms. Thereby, each aforementioned semiconductor chips 11 and 12 will be in the state where it has been arranged back to back. Furthermore, like drawing 3 (b), with the U character type of the aforementioned FPC substrate 10 held, a resin 16 is poured into the interior of the U character mold of the FPC substrate 10, and it is filled up between the FPC substrates 10. And when a resin 16 hardens, the aforementioned semiconductor chips 11 and 12 will be closed with the aforementioned resin 16. Then, the external end-connection child of BGA structure can consist of connecting the solder ball 17 to the external end-connection child 18 by the side of the end of the aforementioned FPC substrate 10, and the semiconductor device 1 of the CSP structure shown in drawing 1 is produced.

[0011] While laying the semiconductor device 1 of the aforementioned CSP structure on the real wearing electrode pad 22 currently formed in the front face of a mother board 21 as shown in drawing 1 in case the semiconductor device 1 of the above composition is mounted in a mounting substrate (mother board), the opposite position of the solder bump 17 who becomes the external end-connection child of BGA structure is carried out. And the solder ball 17 is fused by heating a mother board 21, and it is made to join to the real wearing electrode pad 22. Thus, by performing mounting, two semiconductor chips 11 and 12 carried in the semiconductor device 1 of CSP structure can realize the electrode pad 13 of the FPC substrate 10 and a circuit pattern, and mounting of a semiconductor device [as opposed to / electrical connection will be further carried out to the real wearing electrode pad 22 of a mother board 21 through the solder bump 17, and / a mother board 21].

[0012] Thus, where it changed into the state where are bending the FPC substrate 10 to a U character type after carrying two semiconductor chips 11 and 12 in the FPC substrate 10 by the flip chip method in the semiconductor device 1 of this operation gestalt, and forming, and the laminating of each semiconductor chips 11 and 12 was carried out mutually and the laminating of the two semiconductor chips 11 and 12 is carried out as a result, it will be mounted in a mother board 21, and packaging density improves. Moreover, among the external end-connection children 18 and 19 connected to each semiconductor chips 11 and 12, since the external end-connection child 18 of real wearing is constituted by the solder bump 17 as BGA structure at the end side of a FPC substrate, the external end-connection child when mounting a semiconductor device in a mother board 21 projects to the method of outside [semiconductor chips / 11 and 12], and is not stationed, and he can reduce a component-side product. Furthermore, the laminating of the two semiconductor chips 11 and 12 is mutually carried out in the state of confrontation, since each is carried by the flip chip method to the FPC substrate 10, each semiconductor chips 11 and 12 will not receive restrictions in the size of each semiconductor chips 11 and 12, and they can realize the laminating of the semiconductor chip of the same size. Moreover, in the state of this mounting, it is possible to examine the electrical property of the mounted semiconductor device easily by

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connecting a testing device to the external end-connection child 19 exposed on the upper surface of a semiconductor device.

[0013] Here, as the semiconductor device of this operation gestalt shows to drawing 4, it is also possible to mount other semiconductor devices of the structure same on one semiconductor device mounted in the mother board 21 in the state where the laminating was carried out. That is, it connects to the external end-connection child 19 of electrode pad structure located in the upper surface of the semiconductor device 1 mounted in the mother board 21, other external end-connection children 17, i.e., solder bump, of BGA structure of semiconductor device 1A. By this, electrical connection of the up-and-down semiconductor devices 1 and 1A will be mutually carried out through the external end-connection child 18 (20) and 19, respectively, and electrical connection of the two semiconductor chips 11 and 12 each carried in the up-and-down semiconductor devices 1 and 1A as a result, respectively will be carried out mutually, and mounting will be performed to a mother board 21.

[0014] thus, with the mounting structure which carried out the laminating of the two semiconductor devices 1 and 1A, since a total of four semiconductor chips 11 and 12 will be mounted by the component-side product of about one semiconductor chip, it becomes possible to boil packaging density markedly and to improve. In addition, when not receiving a limit in the height size on mounting, it will also be possible to mount other semiconductor devices of the still more nearly same composition on semiconductor device 1A of the drawing 4 top, and high mounting of packaging density can be realized extremely.

[0015]
[Effect of the Invention] Since a semiconductor device is constituted where a laminating is mutually carried out because two semiconductor chips by which this invention was carried in the insulating substrate bend a substrate to a U character type and form it as explained above, when a semiconductor device is mounted, two semiconductor chips will be mounted where a laminating is carried out, and its packaging density of the semiconductor chip to a mounting substrate improves. Moreover, since the external terminal of a semiconductor device was arranged in one [at least] lateral surface of the lateral surface of the substrate bent to the U character type, while becoming possible to mount an external terminal with solder bump structure, when a semiconductor device is mounted in a mounting substrate, an external terminal projects to a way outside a semiconductor chip, is not arranged, and can reduce a component-side product. Furthermore, it also becomes possible to examine the electrical property of the semiconductor device of a mounting state by performing electrical connection to the external terminal arranged in the lateral surface of another side of a semiconductor device.

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